

# Package Qualification Report

## **EMD1706** 4mm 24-lead QFN Plastic Package



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## 1. Summary

This document outlines the package qualification results for EMD1706, a distributed amplifier housed in a 4x4mm QFN package. The qualification involves evaluating the circuit specified, along with the packaging assembly at Tong Hsing Philippines.

## 2. Reference Documents

MIL-STD-883 "Department of Defense Test Method Standard, Microcircuits"

ANSI/ESDA/JEDEC JS-001 "For Electrostatic Discharge Sensitivity Testing Human Body Model (HBM) - Component Level"

ANSI/ESDA/JEDEC JS-002 "For Electrostatic Discharge Sensitivity Testing Charged Device Model (CDM) - Device Level"

JESD22-A103 "High Temperature Storage Life"

JESD22-A113 "Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing"

JESD22-A104 "Temperature Cycling"

JESD74A "Early Life Failure Rate Calculation Procedure for Semiconductor Components"

JESD22-A118B "Accelerated Moisture Resistance -Unbiased HAST"

## 3. Product Description and Information

EMD1706 is a distributed amplifier designed for high bandwidth applications. It consists of a GaAs amplifier die housed in a plastic overmold 4x4mm QFN, assembled in the Philippines.

### 3.1 Die Information

Die Size: 1.52 x 2.7 mm

Die Thickness: 100  $\mu$ m

Fabrication: 0.15  $\mu$ m e-beam GaAs pHEMT

Foundry: WIN Semiconductors (Taiwan)

Mask ID: DP936

### 3.2 Assembly and Package Information

Package Style: PQFN

Assembly Manufacturer: Tong Hsing (Philippines)

Package Body Dimensions: 4.0 x 4.0 x 0.91 mm

Lead Count: 24

Leadframe Material: C194-FH

D/A Pad Size: 2.65 x 2.65 mm

D/A Plating: One-side Rough Ni PPF

Lead Pitch: 0.5 mm

Lead Finish: NiPdAu

Die Attach: Namics XH9890-6A

Wire Bond: 25  $\mu$ m diameter Gold Wire

Package Material: Sumitomo G770HCD

Marking Method: Laser

## 4. Product Qualification Overview

### 4.1 General Summary

Qualification Vehicle: EMD1706

Lot Numbers/Date Codes: 0103, 0104, 0105

Date Codes: 1843,1844

Test	Condition	Endpoints	Fail/Sample Size	Result
ESD (HBM) JEDEC JS-001	1 positive discharge and 1 negative discharge per pin for each pin combination	Minimum failure from any sample	0/11	Class 0B 150V
ESD (CDM) JEDEC JS-002	Plate charged and discharge with pogo pin per pin	Minimum failure from any sample	0/3	Class C2a 700V
Physical Integrity MIL-STD-883	Solderability Coplanarity	MIL-STD-883 Method 2003	0/15	Pass
Destructive Physical Analysis (DPA) MIL-STD-883	X-ray, C-SAM, Visual Inspection, Die shear, Bond pull	N/A	0/15	Pass
High Temperature Storage Life (HTS) JEDEC SD22-A103A	125°C Ambient Temperature	1000 hours	0/42	Pass
Temperature Cycling JEDEC SD22-A104	Preconditioned Cond. C (-65°C to +150°C) Non-preconditioned Cond. H (-55°C to +150°C)	200 cycles – Read point, continue to 500 cycles	0/42 0/42	Pass
Preconditioning JESD22-A113	MSL1: +85°C, 85% Relative Humidity (RH)	Bake at 125°C for 24 hours Moisture Soak 168 hours 3x Reflow	0/165	Pass
Unbiased HAST JESD22-A118B	Condition A, 130°C, 85% RH, 96 hour	96 Hours	0/42	Pass

## 5. Analysis of Results

### 5.1 High Temperature Storage Life (HTS)

**Test** Follow JEDEC JESD22-A103D to determine the effects of time and temperature, under storage conditions, for thermally activated failure mechanisms. Known good devices are stressed for 1000 hours at 125°C followed by production test re-screening.

**Result** No thermally activated failures were observed at the conclusion of this test.

### 5.2 Preconditioning/Moisture Sensitivity Level (MSL) Classification

**Test** Simulate the effects of board assembly prior to reliability testing with guidance from JEDEC JDS22-A1113. Preconditioning of SMD packages is used to simulate the effects of board assembly prior to reliability testing. This allows reliability testing at the packaged device level on as shippable products with a board assembly simulation. During preconditioning, test samples are subjected to temperature cycling (optional), dry bake, moisture soaking, solder reflow simulation, flux, rinse, dry, and electrical test before reliability testing.

**Result** Parts passed the MSL conditions as per table in Section 4.1. No failures were detected.

### 5.3 Temperature Cycling

**Test** Following JEDEC Standard 22-A104, this test is conducted to determine the ability of components and solder interconnects to withstand mechanical stresses induced by alternating high and low temperature extremes. Permanent changes in electrical and/or physical characteristics can result from these mechanical stresses. An electrical verification test is completed after cycling.

**Result** No visual or electrical failures were found.

### 5.4 Physical Integrity

**Test** MIL-STD-883 guidelines were used to confirm the coplanarity and solderability of the devices to printed circuit boards.

**Result** All samples pass solderability test. Solder coverage on all leads were greater than or equal to 95%. Coplanarity tests pass and are within expected specifications.

## 5.5 Destructive Physical Analysis (DPA)

**Test** Physical integrity testing is completed with X-ray, CSAM, optical inspection, wire bond pull and die shear testing. The appropriate test method is specified by MIL-STD-883.

**Result** All parts examined were within specification. Results point to a process that is repeatable and controlled.

## 5.6 Electrostatic Discharge Sensitivity (ESD) Classification

**Test** Simulates electrostatic discharges that may be placed on the part during handling and assembly of the device. Human Body Model (HBM) testing was performed as per JEDEC JS-001. Charged Device Model (CDM) testing was performed as per JEDEC JS-002.

**Result** ESD results are recorded in the table in section 4.1.

## 5.7 Unbiased HAST

**Test** Unbiased HAST is performed (JESD22-A118B) for the purpose of evaluating the reliability of non-hermetic packaged solid-state devices in humid environments. It is a highly accelerated test which employs temperature and humidity under non-condensing conditions to accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors which pass through it. Bias is not applied in this test to ensure the failure mechanisms potentially overshadowed by bias can be uncovered (e.g., galvanic corrosion). This test is used to identify failure mechanisms internal to the package and is destructive.

**Result** Unbiased HAST results passed. No failures as presented in section 4.1.

## 6. Revision History

**Rev A:** Released on 8th April 2019, Ryan Clement

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